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# Design of an Instrument to Estimate R, L and C Parameters Under Non-Sinusoidal Conditions using FPGA

**Mr K Karneval**
Associate Professor, Department of CSE
Anand Institute of Higher Technology
Chennai, India.
Email: treseofkarnavel@gmail.com

*Abstract: The design of an FPGA-based instrument for nonsinusoidal parameter estimation of R, L, and C passive components is presented in this paper. Designers in the electrical and electronic industries often employ nonsinusoidal waveforms while creating products. Nonsinusoidal signals stimulate all R, L, and C passive components in these circuits. Resistors, inductors, and capacitors all behave differently in a nonlinear signal environment than they would in a sinusoidal signal environment due to their intrinsic nonlinearity. When nonsinusoidal surroundings are present, a problem develops since these components cannot be reliably approximated. The selection of R, L, and C components is critical to designing and controlling electrical and electronic circuits in hybrid filter design and control and digital protection circuits in power systems. So, using a sequential implementation of output error, a Field Gate Programmable Array-based measurement device may properly identify R, Land C components and continuously recalculate the anticipated values of the considered components. The results of measurements may be updated in real-time, memory resources can be better used, and computational steps can be reduced.*

**Keywords— Impedance, equivalent circuits, non-sinusoidal conditions, RLC measurement, real-time estimation.**

## 1. INTRODUCTION

In recent years, electrical and electronic circuits and devices, including analogue and digital components, have become more common in measuring and control applications. Electrical and electronic circuits and devices with analogue and digital components have grown more widespread in measurement and control applications. New measurement methods are needed to decrease those errors.

As a result, we developed a novel R, L, and C measurement methodology parameter estimate approach that is particularly useful when these components function under no sinusoidal situations. Fast measurement rates, affordable measuring apparatus, and high precisions are all provided by this method.

Because of the point-by-point calculations performed by the FPGA in this research, an RLC measurement device based on an FPGA is proposed. The measurement result may be updated anytime a new sample is collected. The proposal aims to achieve an optimum measurement by reducing the hardware resources on the FPGA-based instrument and boosting the measurement rate. Each hardware choice and measurement technique was outlined in detail during the instrument's characterisation. Experimental experiments have shown that the proposed instrument can track time-variant components at high measurement rates.

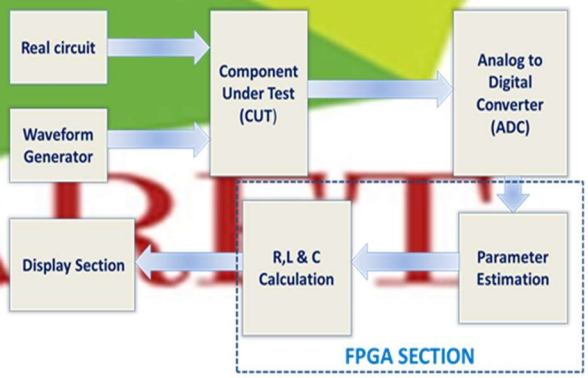


***Fig. 1***. Block diagram of the proposed measurement method.

## 2. INTRODUCTION

Method of Measuring

The following stages form the basis of the measuring concept.

Once the analogous circuit and the operating circumstances are determined, a nonlinear SISO

system may behave like a linear time-invariant (LTI) system. The corresponding circuit in the system identification segment will provide the transfer function H(z).

Assuming a SISO LTI system, the output error model may be used to write y(k) = w(k) + e[(k)], where w(k) is the undisturbed sample output, and e[(k)] is the kth sample added error.

Defined in the discrete-time domain, input x(k) is a function of undisturbed output w(k).

The system transfer function (H(z)) converts the discrete-time domain to the Z domain.

A single parameter set defines all system models in both time and space. It is important to note that the parameters allow the system behaviour to be recreated only inside the established operational context of the parameter estimation section.

The measuring procedure is shown in Fig. 1. Output error parameter estimators are encouraged, as stated in [5]. As stated in [6], an optimisation approach estimates the parameters. Analytical relations are used to determine the system equivalent circuit's R, L, and C parameters. The following is the estimated result for the kth time interval:

$$ypre(k) = H(k) * \hat{\theta} \quad (1)$$

where H(k) = [-y(k-1), -y(k-2),…] and $\hat{\theta}$ is the estimated values of θ.

The error function between the estimated and predicted outputs at the kth interval can be given as

$$e(k) = y(k) - ypre(k) \quad (2)$$

B. Implementation of the OE Algorithm

It is feasible to give details that the mean-square error solution to the problem of minimizing Equation (2) can be given as

$$\hat{\theta}_N(k)=(H^T(k)H(k))^{-1}H^T(k)y(k)=P(k)H^T(k)y(k) \quad (3)$$

Finally it can be written as

$$\hat{\theta}(k)= \hat{\theta}(k-1) + L(k)[y(k) - H(k)\,\hat{\theta}\,(k-1)] \quad (4)$$

Where,

$$L(k) = P(k-1)H^T(k)[I + H(k)P(k-1)H^T(k)]^{-1} \quad (5)$$

The solution given in Equation (4) is illustrated, in a graphical form, in the block diagram given in Fig. 2.

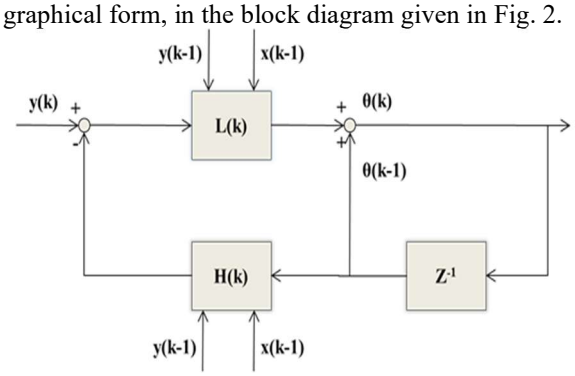


***Fig. 2.*** Graphical depiction of the implementation of the OE algorithm

C. Implementation in an FPGA

Sequential implementation in suggested FPGA-based design is being measured in terms of output error algorithm adoption ease using the following two figures of merit:

1) The minimal number of samples saved in the memory is determined by the amount of memory required.

2) The amount of operations required to get the specified parameter set values is the computational load.

A first-order model is used for the predictable analysis. Because of this, it is vital to investigate how to estimate coefficients, which are used in the computation of the R-L-C components based on the estimated parameters.

To make full use of the observation and sampling times, a total number of samples equal to the combined duration of both are collected during observation.

As seen in Fig. 3, the sequential implementation of the estimate method is used to calculate the coefficients.

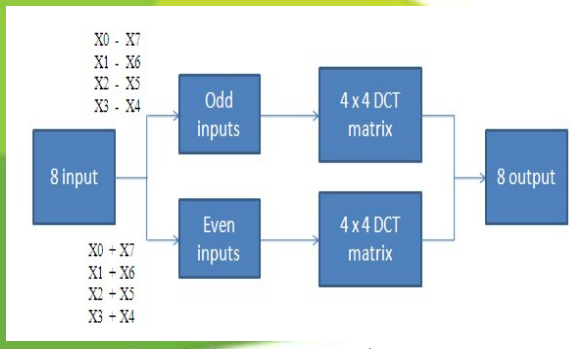


***Fig 3.*** Decomposed DCT

The 8 x 8 DCT matrix is multiplied by the eight input values in an 8 point DCT. Sixty-four multipliers are needed to achieve all eight outputs. Minimising the multipliers' utilisation by 50% is possible by adding one pre-processing unit to decons DCT architecture ( only 32 multipliers used). We solely employed adders in the pre-processing unit. Ultimately, we can lower the complexity of the hardware.

## 3. PERFORMANCE DESCRIPTION

A suitable simulation environment was used to conduct a characterisation portion of the study. This section aims to estimate the measurement technique's static and dynamic performance and provide the hardware requirements for the extra implementation portion of the project. The basic mean accuracy, sensitivity, and repeatability alltruct play a role in static performance. It is discussed in terms of reaction

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and settling times for dynamic performance. An important consideration in deploying a data acquisition system (DAS) is its internal noise and resolution and any probe noise that may develop due to poor connection quality. This DAS effective number of bits is used to simultaneously measure all the noise sources.

Matlab's platform runs various numerical tests as part of the characterisation process. It is feasible to do the following in this situation:

Exciting non-sinusoidal signals may be generated via (1)

determine which R, L and C passive components are needed

estimate the output of each component about the signals that are stimulating them

A simulation of FPGA-based computing taking into account the number of bits and an evaluation of component performance taking into account the fixed-point arithmetic of FPGA are two of the steps in the process.

Multiline stimulation signals represent various nonsinusoidal signals in the tests, and R, L, and C circuits are randomly produced. Generation of Multisine signals by choosing the number of tones [1–50] and also the frequency contents [50 Hz–100 kHz] as well as the phases [02]. The circuit for the device under test is sketched out, with arbitrary resistance, inductance, and capacitance values ranging from [1 – 1 M], [1 H–1 mH], and [100 pF–100 F].

In every test, once the stimulation(non-sinusoidal) signal and the R, L, and C passive components combination are chosen, the associated output signal is calculated. Then, the sequential evaluation method starts, and the FPGA simulation atmosphere forces the hardware resources to work within the same fixed point calculating conditions permitted by the FPGA.

Every test is repeated by considering various values of the resolution (number of bits) of the analogue-to-digital converter (ADC): numbers of bits that can be varied from 6 to 16 have been considered. A complete and different test is executed for every resolution (number of bits). In every test, a sampling frequency has been considered as 1MHz, and a maximum observation time of 3s has been considered.

For every test, the subsequent figures of merit are calculated:

1) The difference between the mean value of the R, L, and C measurement results in percentage provided by the algorithm and the R, L, and C measurement results provided by the imposed one.

2) The experimental standard deviation σ of the measurement results in percentage.

3) The settling time (Tsett): the time was taken of the system to reach a threshold of ±5% of the steady-state response. The steady-state response is looked like the output of the nonsequential OE parameter estimation algorithm operating on a complete observation time of 1s.

4) The response time (Tres): the time was taken of the system to reach a threshold of 90% of its steady-state response. The steady-state response is looked likely to the output of the nonsequential OE parameter estimation algorithm operating on a total observation time of 1s.

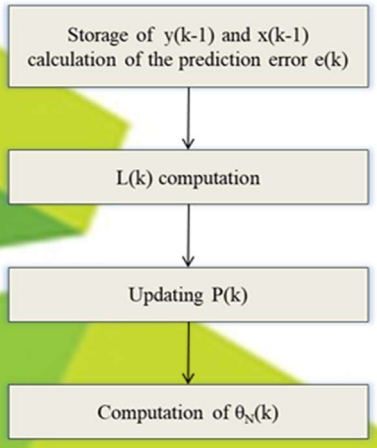


***Fig. 3.*** Logical steps for the estimation algorithm.

By using Horner's rule, the more powerful operator of multiplication is reduced to a simple shift and addition operation. As a result, less electricity is used. There are many examples of this. Consider the cosine coefficients C and G, c *X = 25 +1 (X) = (24 (3) + 5 (X) and g *X = 23 +1 (X) = 22(3) (X) and the common terms they share are 3X. The terms 1X, 3X, 5X, and -1X are shared by the cosine basis and are used to calculate the partial outputs. Precomputing units are what we refer to as in this context.

## FPGA BASED INSTRUMENT

The following sections detail the instrument's hardware and software requirements for the proposed FPGA-based passive components measuring approach.

A. Devices and Hardware

The following parts make up the hardware design phase: 1) the probes for voltage and current.

The digital to analogue converters Three and four are FPGA-based processing and communication.

A digital-to-analogue converter (ADC) converts the analogue voltage and current signals from the component under test. The ADC section must handle the bandwidth and output range of the probes.

ADC is responsible for the collection of data in this area. It's a two-channel system. The ADC uses a sequential approximation register [8] for its operation.

An FPGA chip is used to calculate the properties of passive components. A Xilinx SPARTAN 3 device is employed in particular [9]. It is a fixed-point FPGA chip that has been chosen. Seven hundred thousand system gates, 1472 computing logical block arrays, 13248 logic cells, 92000 distributed RAM bits, 360 000 block RAM bits, 20 specialised multipliers, and 372 user I/Os are all required characteristics of the FPGA device under consideration.

4) An RS232 data port has been used to finish the connection part. For a first-order R, L, and C model, the RS232 circuit standard allows a maximum baud rate of 400 kb/s. Because of the ease with which it may be connected to a computer, an RS232 data connector was chosen (PC).

B. Firmware

The firmware computing part consists of four main blocks: 1) signal acquisition, 2) parameter set computation, 3) R, L, and C estimation, and 4) data transmission.

1) The serial word coming out from the Analog to Digital Converter block represents the sampled signals obtained [i.e., x(k) and y(k)].

2) In the computing section, in the beginning, the stage itself, the user can create delusions of some external selectors, the types of components and the model order of the selected components. The transfer function's structure and the number of estimated coefficients are defined with these details. When a new sample is acquired, a processing cycle starts to estimate the coefficients and estimate the predicted output.

3) The passive component model selected by the user drives the R, L, and C estimation part. The passive component parameters are computer from coefficient values with the help of Analytical relationships. The sequential implementation of the measurement algorithm requires the upsample and downsample parts in the computation section. Specifically, because the Analog to Digital Conversion section operates at a rate of 1 MS/s, whereas the FPGA can access data with the highest frequency of 400 Mflops, the upsample part permits changing the rate of the computation section concerning the Analog to Digital Conversion part. During this means, all the required operations can be controlled in a single time clock of the ADC of 1µs. The downsample block permits the computed results as per output rate.

4) The transmission section gives the passive components parameters using a serial port that will operate in the baud rate from 115200 to 400000 b/s.

C. Measurement Method

The FPGA device has built a suitable measuring approach in light of the prior characterisation findings. The settling time may be defined as the amount of time it takes for a reaction to stabilise. The worst settling time recorded in the preceding characterisation portion was evaluated to be 50 ms or less competent. When the instrument achieves a steady state, the estimating process essentially ends.

While the algorithm is taking the measurements, the value of P is reduced (k). Towards Zero, the measuring method converges to its ultimate values. The R, L, and C values cannot be changed.

The instrument's steady-state response is attained when the P(k) matrix is close to zero. The P(k) matrix is then reinitialised to the P0 value every 50 ms to estimate the coefficients continuously. The new parameter estimate process is formed faster, time response is sped up, and determined R, L and C values are scaled-down by not resetting them to zero.

Regarding the measurement's outcome, R, L, and C are represented by 40b for every sample time Tc. The updated R, L, and C values must be provided over the serial port.

The first-order model means that 80b must be outputted over the serial port for each estimate update. Due to the serial port being configured at 115200b/s, every 1ms, the measurement output is updated with new results every time the Tc sampling time is performed.

D. Simulation Result

Details of the frequencies and magnitudes of the tones involving the stimulus signal1 and stimulus signal2 are reported in Table I.

Table II Passive component values for different stimulus signal

| STIMULUS SIGNAL 1 | | | | | | |
|---|---|---|---|---|---|---|
| Frequencies[Hz] | | 50 | 150 | 350 | 450 | 550 |
| Magnitude (voltage) | R | 2.60 | 1.56 | 1.04 | 0.65 | 0.13 |
| | L | 1.58 | 0.94 | 0.63 | 0.39 | 0.08 |
| | C | 45 | 27 | 18 | 11.3 | 2.3 |

| STIMULUS SIGNAL 2 | | | | | | |
|---|---|---|---|---|---|---|
| Frequencies[Hz] | | 50 | 500 | 600 | 700 | 800 |
| Magnitude (voltage) | R | 2.3 | 1.38 | 0.92 | 0.69 | 0.58 |
| | L | 4.8 | 2.88 | 1.92 | 1.44 | 1.20 |
| | C | 27 | 16.2 | 10.8 | 8.10 | 6.75 |

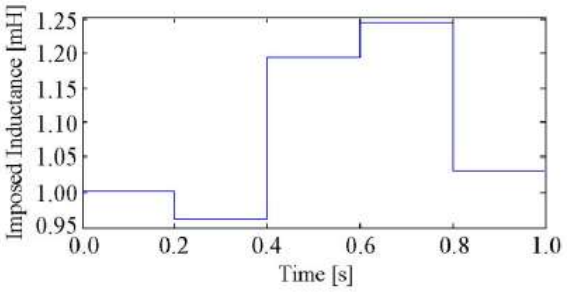


***Fig.4.*** Inductance values in RL series circuit

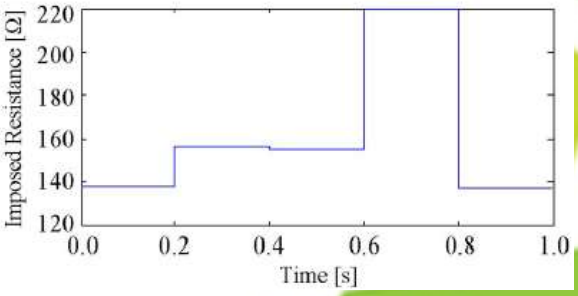


***Fig. 5.*** Resistance values in RL series circuit.

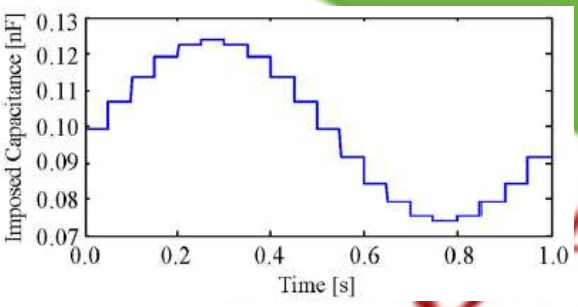


***Fig. 6***. Capacitance values in RC parallel circuit

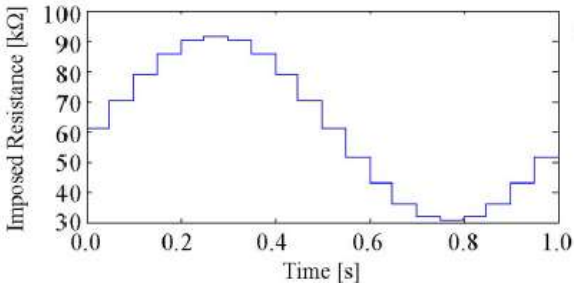


***Fig. 7.*** Resistance values in RC parallel circuit.

## 4. CONCLUSION

FPGA-based R, L and C passive component parameters estimate instruments have been reported for non-sinusoidal circumstances. The proposed method has several benefits because of point-by-point signal processing, decreased memory resources, and relatively low computing overhead. In a simulated setting, a change of the measuring approach allowed for improved procedure. Techniques that may enhance measurement reaction time, decrease memory, and increase bandwidth will be used in future instrumentation development efforts.

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