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Design of Parity preserving BCD adder using Reversible Gate Logic.

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Abstract : Nanotechnology, optical computing, quantum computing, and lw-power CMOS architecture are all using reversible logic circuits. In binary-based electronics, low-power and high-speed adder cells (such as the BCD adder) are employed. Binary addition is a basic operation in almost all digital circuits. All other arithmetic operations may be synthesized from it. The major problem now is to reduce the power consumption of adder circuits while retaining excellent performance across a variety of circuit configurations. For error detection in digital systems, parity preservation is also an option. BCD adder design that is fault resistant and preserves parity is suggested in this paper. Reversible logic gates such as IG, FRG, and F2G are used in the suggested technique to reduce the circuit's power consumption and quantum cost. It is compared to the present circuit in terms of the number of constant inputs and garbage outputs, the latency, and the quantum cost.

Keywords— BCD Adder, Reversible Logic, Double Feynman Gate, Islamic Gate (IG).

1. INTRODUCTION (*Heading 1*)

Fault tolerance is the ability of a system to function successfully even if some of its components fail.. Fault detection and rectification are simplified when the system is built using fault-tolerant components. Parity is used to provide fault tolerance in a wide variety of systems, including communications. As a result, the design of fault-tolerant reversible systems in nanotechnology will increasingly rely on parity-preserving reversible circuits. A network of gates will be parity-preserving as long as each gate is. There have been a few proposals for logic gates that preserve parity. If the EXOR of the inputs equals the EX-OR of the outputs, then a reversible logic gate is parity-preserving, meaning that the parity of the input and the output stays constant. The NFT gate, Islamic Gate (IG), Double Feynman Gate, F2PG, and PPPG are some of the parity-preserving reversible logic gates that are important in this subject. It is also a reversible logic gate that preserves parity.

A. Double Feynman Gate (F2G)

A 3*3 Double Feynman gate is shown in Fig. 1 below. (A, B, C) is the input matrices, while (O) is the output matrices (P, Q, R). P establishes the results to be produced.

The following equations are equivalent: =A, Q=A or B, R=AxorC. The double Feynman gate has a quantum cost of 2.

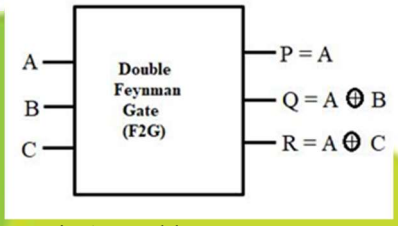

Fig 1: Double Feynman Gate

B. Fredkin Gate

Three-by-three Fredkin gate is shown in Fig 2. (A, B, C) is the input matrices, while (O) is the output matrices (P, Q, R). P=A, Q=(A'B) xor (AC) and R=(A′ C) xor (AC) define the output (AB). A Fredkin gate has a quantum cost of 5. The logic circuit for this 3x3 gate is shown in the image. It has a five-qubit cost. Using it as a Multiplexer is an option. From the same control input A, this gate is just two multiplexers that have been switched (permuted).

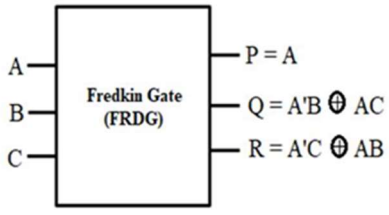

Fig 2: Fredkin Gate

C. IG GATE

Figure 3 depicts an IG gate with four sets of four inputs (A, B, C, and D), four sets of four outputs (P, Q, R, and S), and a binary value (P = A, Q = B, R = C, and S = D).

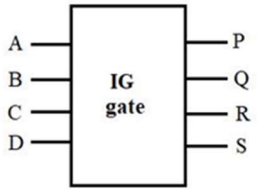

Fig 3: IG Gate

The following is a diagram outlining the paper's structure. Reversible logic and BCD adder design are discussed in Section-II. Section III focuses on

the work that has been suggested Section IV includes the design implementation and simulation results. Section V concludes the discussion.

2. RELATED WORK

Compared to other ripple carry adders, Thapliyal H,et.al. [1]'s novel design of the reversible BCD adder uses a ripple carry adder with reduced logic depth (delay) and is optimised for input bit count and garbage output count. There was a better design for this in the work of Anshul Singh et al.

Binary Coded Decimal (BCD) addition and subtraction is an efficient method that does not need any additional hardware. Both signed and unsigned numbers may be used in the design. An efficient reversible logic implementation of BCD adder adders in terms of gates and garbage outputs has been presented, as well as a Carry Skip BCD Adder. [3] Reversible design BCD adder was designed by Naderpour F. et al [4] with the goal of reducing the circuit's depth. His name is Ashish Kumar. Md. Biswas et al. Using reversible conservative logic, James, R.K. Shahana, et al. (2007) suggested a technique for fast decimal addition (QAD) appropriate for multi-digit BCD addition. Only reversible fault tolerant Fredkin gates are used in the design. For n-bit binary numbers and m-decimal BCD numbers, M.K. Thomsen and R. Gluck [7] have developed a comprehensive set of reversible half- and full-adders. By H.M.H. Babu and A.R. Chowdhury [8], an innovative reversible logic synthesis technique known as the "reversible binary coded decimal (BCD) adder" was presented for the first time. A TSG gate-based reversible logic version of the traditional BCD adder and the carry skip BCD adder was suggested by Himanshu Thapliyal, et al. [9].

Reversible computing for low-power computing has received a lot of attention from researchers, according to a literature review. The goal of this study is to construct a fault-tolerant BCD Adder using an optimised parity-preserving BCD Adder. To decrease the number of garbage outputs and at the same time lower the number of constant inputs, the major design attention will not only be on the design but also on the usage of a minimal number of reversible gates. Reduced trash production is an indirect indication of decreased hardware complexity. The switching activity will automatically decrease when the hardware is reduced, assuring less power consumption while also improving speed. It is possible to design sophisticated circuitry to accomplish ALU operations with little power consumption thanks to this energy efficient cell.

A. BCD Adder

Adding two BCD digits in parallel, a BCD 1-digit adder outputs the sum digit in BCD as well as the correction logic required. Adding two BCD numbers requires a BCD adder, a combinational circuit. The input and output must both be binary coded decimal for the BCD adder to work. Using two 4-bit binary integers as input, it will return a single output value. Both inputs must have a value between 0000(0) and 1001 as their range (9). After that, we'll have an output that's no more than 9. Using a BCD adder, if the total is higher than 9, the output must be corrected by adding 0110(6) to the sum. Conventional BCD adders use a lot of power and have a long delay. C0 is used to represent the input carry in the reversible BCD adder [10], OC is used to represent the 4 bit adder's carryout, and OC is used to represent the 1-digit BCD adder's output carry. 1ancilla input bit and zero trash outputs are available in the current BCD adder architecture. The suggested reversible BCD adder with input carry has a quantum cost of 70. Current BCD reversible adders are limited by their complexity and the large number of possible configurations for their reversible gates.

3. PROPOSED BCD ADDER

It is built utilising parity reversible gates to ensure that the BCD Adder will retain its original parity. A parity-preserving BCD adder is more secure for data transfer than a standard BCD adder. Reversible logic gates with parity preservation have the extra feature that the input parity and the output parity are the same. Parity

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reversible gates are used to create a BCD Adder that preserves parity. Figure 4 depicts the three-step process used to create the BCD adder. Parity-preserving reversible gates like the IG gate are used in the initial stage to build the entire adder circuit. Two IG gates are needed to accomplish it. Second, cascading the adder circuits, the 4-bit ripple carry adder is built using the specified IG gate.

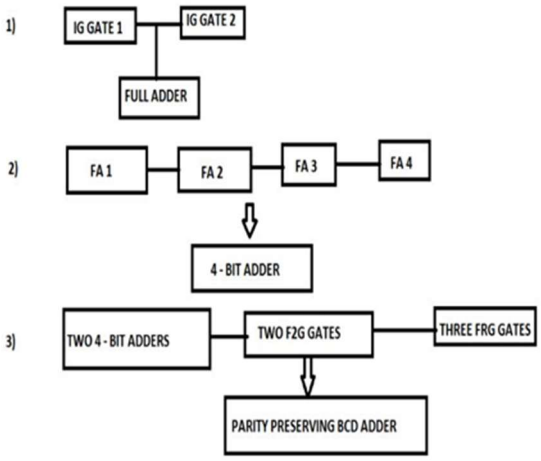

Fig. 4: Flow chart of design of proposed BCD Adder

A normal BCD adder idea is used in the final phase of the design process, with the main distinction being the use of parity reversible gates in the proposed architecture. Two 4-bit ripple carry adders, two feyman double gates, and three fredkin gates were used in the logic simplification.

A. Full Adder using IG Gate

The full adder circuit is used to add three bit binary number and the standard Boolean expression is:
Sum = A ⊕ B ⊕Cin
Carry = (A ⊕ B) Cin⊕ AB

The IG gate based implementation is shown in fig. 5. As observed the architecture uses two IG gate which along with required input and outputs have two constant input as logic 0 and three garbage shown as G1, G2 and G3.

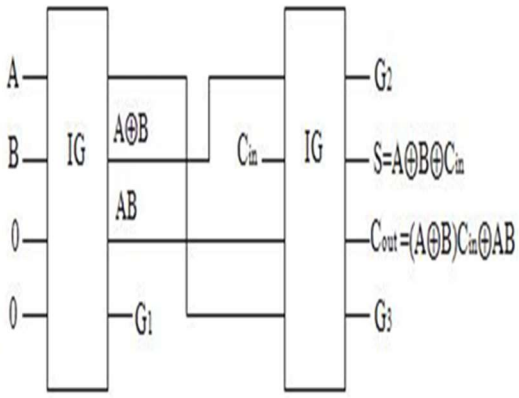

Fig 5: Two IG as Full Adder

The expressions for garbage outputs: G 1= B′ A, G2 = A⊕ B and G3 = Cin A ⊕Cin′ B.

B. Design of 4-Bit Ripple Adder

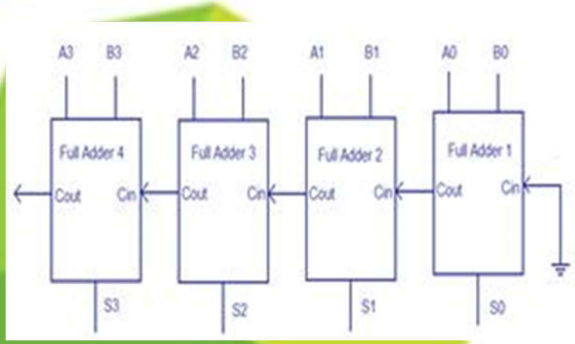

Fig 6: Block diagram of 4-Bit Ripple Adder

The 4-bit ripple carry adder design is shown in fig. 6. It uses four proposed full adder (fig. 5) which long with required input and outputs have 8 constant inputs and 12 garbage outputs.

C. Parity preserving BCD Adder

Reversible logic gates with parity preservation have the extra feature that the input parity and the output parity are the same. Two 4-Bit Ripple Carry Adders, two Feyman Double Gates, and three Fredkin Gates are required to construct the suggested parity-preserving BCD Adder, along with a few more parity-preserving reversible gates (see Fig. 7).

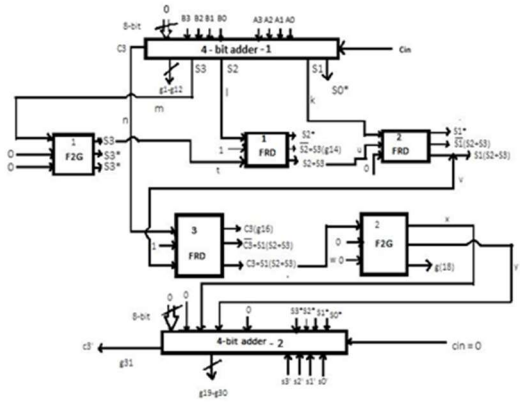

Fig. 7: Proposed Parity Preserving BCD Adder

The working of each module in proposed BCD adder is detailed below as follows:

(i) 4-BIT RIPPLE ADDER-1

'A' and 'B' denote the two 4-bit binary numbers that make up the block's BCD numbers. These two inputs are combined with an 8-bit constant input of logic 0 to form a 4-bit parity preserving reversible adder. Carry is considered to be 0 in this 4-bit adder. S3, S2, S1, and S0* are the outputs of a 4-bit adder, whereas the remaining outputs are g1-g12, which are essentially unused bits.

(ii) F2G -1

S3 of 4-bit adder -1 is given as one of the inputs of F2G-1 whereas other two inputs are default 0. It has three inputs s3,s3* and s3*.

(iii) FRD-1

S2 from 4-bit adder1 is given as one of the inputs and second input s3 from F2G1 is given. The third input is by default 1. Therefore FRD-1 outputs are s2*,s2`+s3(g14),s2+s3.

(iv) FRD-2

S1 from 4-bit adder-1 is given as one of the inputs for FRD-2, output s2+s3 of FRD-1 is given as another input to FRD-1 and third input is default 0. Therefore outputs of FRD-2 are s1*,s1(s2+s3),s1(s2+s3).

(v) FRD-3

C3 is given as one of the inputs, output s1(s2+s3) of FRD-2 is given as another input to FRD-3 and third input is default 1. Therefore outputs of FRD-3 are c3(g16), c3`+s1(s2+s3),c3+s1(s2+s3).

(vi) F2G-2

The output C3+S1(S2+S3) of FRD-3 is given as one of the inputs to F2G-2 and other two inputs are by default. The outputs of F2G-2 are X,Y,g(18).

(vii) 4-BIT RIPPLE ADDER-2

The two outputs X, Y of F2G-2 is given as inputs and other inputs are s3*, s2*, s1*, s0*,0,0. The output of 4-bit adder-2 will be obtained in the form of sum and carry.

From the architecture, it can be observed that the number of inputs is equal to number of outputs which obeys the law of reversible principle.

4. SIMULATION RESULTS

The synthesis of proposed BCD adder is done using

ISE simulator of Xilinx and the simulation with the help of Modelsim-SE of mentor Graphics. The simulation of each block of proposed adder is shown in fig. 8 to fig. 10.

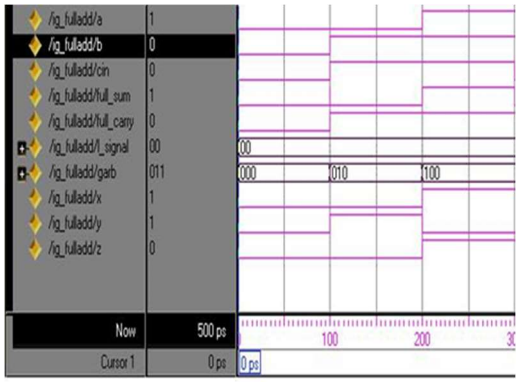

Fig 8: IG Gate as a Full Adder

Fig. 9: 4-Bit Adder using IG Gate as Full Adder

Fig 10: Parity Preserving BCD Adder

From simulation results, it can be observed that the number of input and output lines are equal as well as the results are also satisfied for each operation.

5. CONCLUSION

As our everyday lives become more enmeshed in mobile technology, power consumption has emerged as the most pressing issue facing today's devices. We wanted to learn more about Reversible Computation and how it may be used to make gadgets more energy efficient so that they have a longer useful life. When it comes to computer hardware, the BCD Adder is an essential part of the arithmetic circuitry. When BCD Addition is being conducted, this unit is expected to use the greatest power. Fault tolerant gates Fredkin, F2G, and IG have been used to create a parity-preserving BCD Adder circuit that is reversible.

REFERENCES

[1] Thapliyal, H.; Ranganathan, N., "A new reversible design of BCD adder," Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011 , vol., no., pp.1-4, 14-18 March 2011.

[2] Anshul Singh, Aman Gupta, Sreehari Veeramachaneni, M.B. Srinivas, "A High Performance Unified BCD and Binary Adder/Subtractor," isvlsi, pp.211-216, 2009 IEEE Computer Society Annual Symposium on VLSI, 2009.

[3] Biswas, A.K., M.M. Hasan, A.R. Chowdhury and H.M.H. Babu, 2008. Efficient approaches for designing reversible Binary Coded Decimal adders. Microelectronics Journal, 39(12):1693-1703.

[4] Naderpour, F.; Vafaei, A.; , "The Design of Reversible BCD Digit Adders: Decreasing the Depth of Circuit," Communications and Information Technologies, 2008. ISCIT 2008. International Symposium on , vol., no., pp.310-314, 21-23 Oct. 2008.

[5] [5] Ashis Kumer Biswas, Md. Mahmudul Hasan, Moshaddek Hasan, Ahsan Raja Chowdhury, Hafiz Md. Hasan Babu, "A Novel Approach to Design BCD Adder and Carry Skip BCD Adder," vlsid, pp.566-571, 21st International Conference on VLSI Design (VLSI Design 2008), 2008.

[6] [6] James, R.K.; Shahana, T.K.; Jacob, K.P.; Sasi, S., "Quick Addition of Decimals Using Reversible Conservative Logic," Advanced Computing and Communications, 2007 (ADCOM 2007) International Conference, vol., no., pp.191-196, 18-21 Dec. 2007.

[7] [7] M.K. Thomsen, R. Gluck, Optimized reversible binary-coded decimal adders, Journal of Systems Architecture, pp 697-706, (2007).

[8] [8] H.M.H. Babu, A.R. Chowdhury, Design of a compact reversible Binary Coded Decimal adder circuit, Elsevier J. Syst. Archit. 52 (5) (2006) 272– 282.

[9] [9] Himanshu Thapliyal, Saurabh Kotiyal, M. B. Srinivas, "Novel BCD Adders and Their Reversible Logic Implementation for IEEE 754r Format," vlsid, pp.387-392, 19th International Conference on VLSI Design held jointly with 5th International Conference on Embedded Systems Design (VLSID'06), 2006.