

VLSI Design Based Delay and Power Performance Comparison and Analysis of Multipliers

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Abstract:

Recently, the problem of power dissipation has become more important in VLSI design. The multiplier is a major drain on resources. The multiplier is a basic operation in arithmetic. This article examines a variety of multipliers at the algorithmic, circuit, and layout levels. The multiplier schematic was designed using TANNER TOOL. It has been possible to increase the speed and area of multipliers by utilising Vedic mathematics for multiplication. Vedic mathematics' "Ni khilam sutra" formula can multiply large numbers. One of the primary objectives is to increase speed while simultaneously decreasing power, area, and delay.

Keywords— Vedic Multiplier, VLSI, Sutra, Power Performance.

1. Introduction

All logical arithmetic procedures need the use of multiplication, a basic arithmetic operation. In a DSP system, the processing power is dictated by the system's multiplication capabilities. Power consumption is an important consideration in VLSI design. The power consumption of circuits rises in lockstep with the complexity and number of transistors on a chip. Potable designs that use more power have a shorter lifespan since the power source runs out faster, requiring more power from the battery. It's becoming more and more important to reduce power consumption while yet retaining great performance in mobile computing devices. Techniques like the array multiplier, Wallace tree multiplier, and Booth multiplier have all been suggested in the literature as fast multiplication methods for VLSI implementation. This page goes into considerable detail about the different methods' technological foundations. A number of logic types may be used to create low-power, high-speed VLSI. VLSI design is heavily influenced by power, area, and latency. The number of low-power, high-speed logic designs has exploded, and each of these logic designs offers unique benefits in terms of both speed and power.

2. Materials and Methods

2.1 Objective

A good multiplier strives for both high speed and low power consumption. Physically, it should be a tiny object. As a crucial part of arithmetic processing units, multipliers are in high demand due to their speed and low power consumption. Minimizing the number of operations in a multiplier design helps to reduce dynamic power, which makes up a significant percentage of total dissipated energy. Multipliers in VLSI have already seen a great deal of research effort.

3. Methods and Performances

3.1. Array multiplier:

One way to think of it is as an array multiplier is a combinational multiplier that has an array structure to it. Two binary numbers may be multiplied in one micro-operation using a combinational circuit that creates the product bit alliance. This is a quick way of multiplying two numbers since the only delay is caused by signals travelling through the multiplication array's gates. Consider the array multiplier of two m-bit binary integers A and B.

Multiple AND gates in parallel create many sums in parallel. For the $n \times n$ multiplier to function, it needs as many full adders, half adders, and AND gates as there are bits in the n th operand. $2n+1$ is the maximum delay that an array multiplier can have. The array multiplier expands the available data.

Although this multiplier is faster, it also consumes more power and has a longer delay. A larger number of gates is also required, increasing the array

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multiplier's volume and cost. As a consequence, although it has a fast multiplier, the hardware complexity is very large.

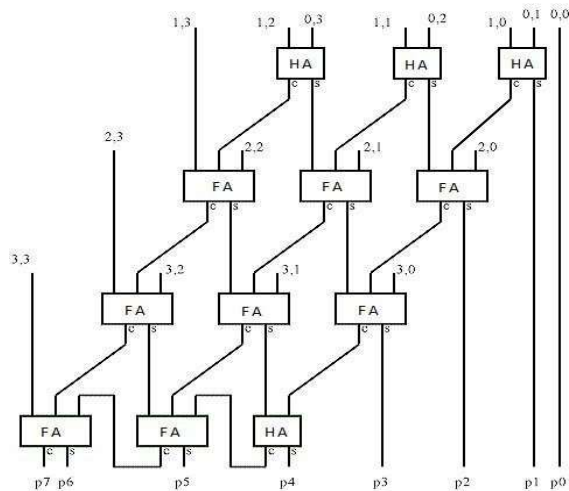


Fig1 structure of array multiplier 4.2.Wallace tree multiplier:

Wallace found an efficient way to multiply two numbers quickly. Use this three-step process to multiply two integers. We can quickly sum the bit products by dividing the matrix into two rows. In order to complete the bit product matrix, we'll utilise a fast adder on these last two rows. One-bit full adders add three bit signals, and the result is fed into a three-input Wallace tree circuit, where the output signal is fed into a full adder one bit higher in the chain, where the carry output signal comes out.

Decrease the multiplier's performance by fewer unfinished products. For example, the recording booth recording multiplier scans three boys at a time to reduce imperfect products. These three bits consist of the two bits from a pair plus a third bit from the high order bit of an adjacent lower order pair. For each three-bit element in the array's adder cells, booth logic is used to analyse and convert it into a set of control signals that the adder cells may use to guide their activities.

It accelerates multiplication by doing multiple computations at once. The Booth technique takes use of the fact that adder subtractors are both quicker and smaller than standard adders. Booth multiplication, on the other hand, often has a lower latency than array multiplication. In contrast, the delay performance of the booth multiplier is data-dependent.

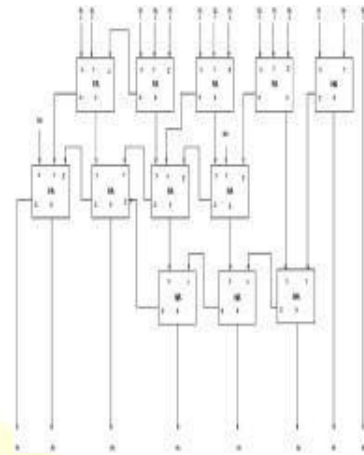


Fig2 structure of Wallace tree multiplier 4.3.Booth multiplier:

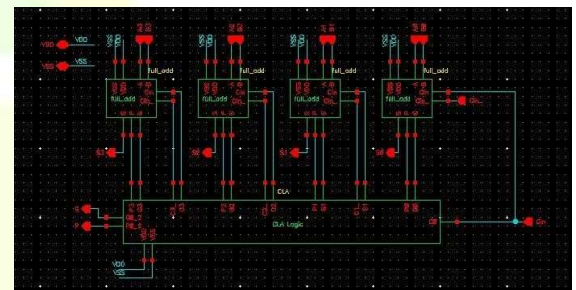


Fig3 structure of Booth multiplier 4.4.Vedic multiplier:

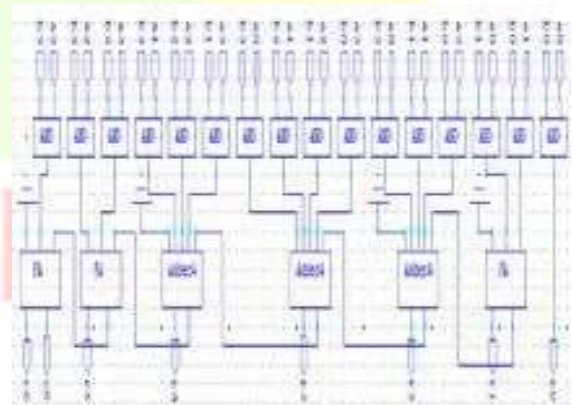


Fig4 structure of vedic multiplier

Vedic mathematics, a centuries-old Indian methodology, draws on 16 sutras to create a unique arithmetic calculating method (formulae). Vedic mathematics has the advantage of simplifying complicated calculations that would otherwise be

necessary in traditional mathematics. It is said that vedic formulae are based on the same fundamental principles that underpin human thinking. Vedic mathematics uses a method based on arithmetic concepts that allows for more rapid implementation. Several helpful algorithms may be found here that can be used in a wide range of technical areas, including computer science.

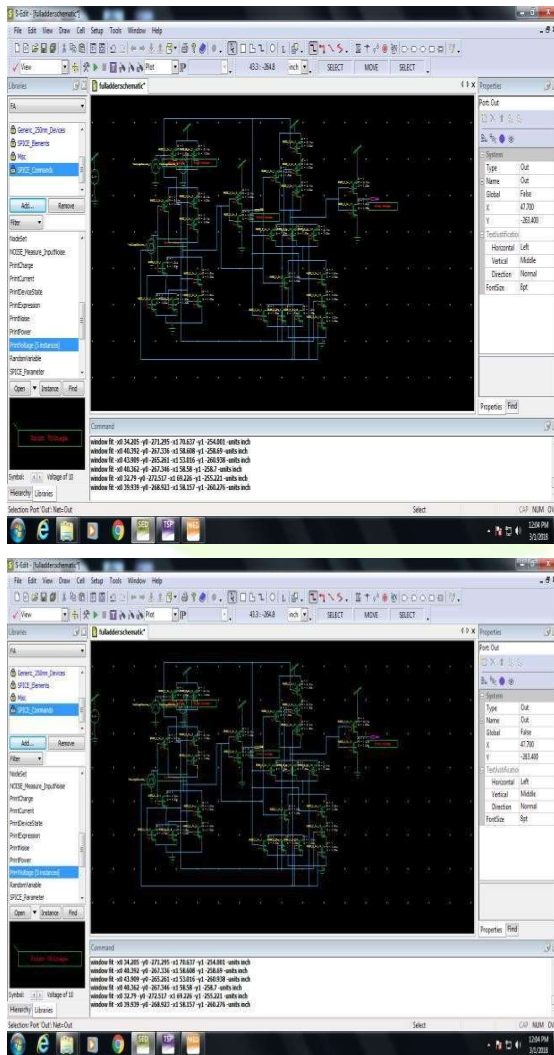


Figure 5: waveform for full adder

4. Comparative Analysis of Multiplier

S.No	MULTIPLIER	DELAY	POWER
1	Array	3.10sec	3.75mW
2	Booth	2.65sec	0.95mW
3	Wallace tree	4.24sec	11.65mW
4	Vedic	1.62sec	0.07uW

Table 1: Comparative analysis of Multiplier

5. Conclusion

When working with DSP applications, multipliers are often need to be used. These multipliers are often used in microprocessors, DSPs, and data processing applications. Array, Booth, Wallace, and Vedic multipliers were designed and implemented at the circuit level as a part of this research. Using Verilog code and the tanner tool, these circuits are simulated and synthesized, and the output waveforms are recorded. During the whole design process, the power was multiplied by the multiplier. Because of its superior performance in all the previously stated categories, the Vedic multiplier beats out all other techniques.

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