

An IGSVL and SGSVL FinFET 6T SRAM-based novel power reduction technique

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Abstract:

The development of future portable integrated circuits will need to focus on power optimization. As the consequence of continuous current flow, the rise in leakage current in VLSI circuits has recently emerged as a significant issue to solve. It is feasible to reduce the threshold voltage while still decreasing leakage, as long as you don't compromise the other design objectives. An integrated circuit's ability to operate at low power will be more essential in the future. Using current scaling technologies, it seems that Fin FET may potentially be a more practical choice for bulk CMOS. Fin FETs are said to be better than ordinary CMOS transistors since they are double gated. For minimizing power usage, you should use twin gates that are driven simultaneously or independently. In this research, T-Spice is used to install Fin FETs in 45nm SRAM cells that were produced using SRAM cells made in various process technologies to reduce leakage in the circuits under discussion.

Keywords— Fin FET, Shorted Gate, Power Reduction Technique, 6T SRAM

1. Introduction

Bulk MOSFETs have gate control that is inferior than FinFETs, and thus, FinFETs have been seen as a potentially interesting future technology [1]. An approach that enables for the fin width to increase just in proportion to the fin height while still providing the 2nm gate width would be considered a quasi-planar construction for Fin FETs (fig. 1) [3]. In Fin FETs, the gate voltage has greater control over the channel since the SCE is higher. Subthreshold leakage current (SCL) may be reduced by using a device with a lower SCE, such as a Fin FET. In a Fin FET, the second gate is linked to the first gate in the opposite way. The two types of Fin FETs on the market are the CDDG and the IDDG. To make SCE better in CDDG, the two gates are connected. In contrast, to reduce leakage current in IDDG, the V_{th} is regulated by providing a bias voltage to the second gate. A significant part of the chip space is taken up by SRAM arrays. In a single cache cell, a significant amount of total power consumption in the CPU may be reduced since the capacity of the on-chip memory has increased because of the leakage current reduction. The main problem with SRAM is standby power consumption, which is most prominent when inactivity is extended to lengthy periods and activity is limited to short periods.

increasing the threshold voltage threshold voltage and read margin control using a bigger threshold voltage In this work, we propose a technique for minimising the current leakage in Fin FET SRAM cells using a low-power method.

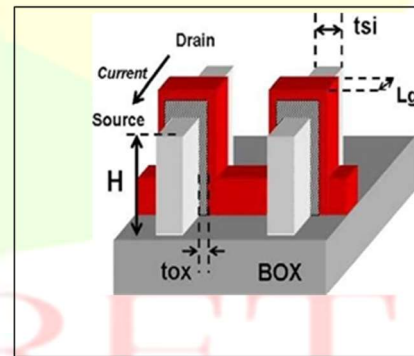


Figure 1. Structure of FinFET

The remainder of the paper is organised as follows: Leakage current is covered in Section II. The proposed low-power SRAM cell properties are given in Section III. In the last section of this paper, we will provide our results and conclusions..

2. Fin FET - 6T SRAM cell operation and its leakage mechanism

The twin gate Fin FET SRAM cell architecture is a more preferred alternative to the current standard. CMOS (Complementary Metal Oxide Semiconductor) is utilized

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because to the self-alignment of the opposite sides of the gates. Leakage is reduced by decreasing the supply voltage threshold voltage (V_{th}) and Fin height. To improve performance, it is important that the SRAM cells need low power consumption and short access times. For that reason, Fin FIT-based SRAM cells were selected, which have low power consumption and quick access times. In SRAM cells, there are three different modes of operation: standby, read, and write. Set it too standby. To disconnect the cell from the bit lines, the access transistors M5 and M6 must be enabled. The two cross coupled inverters retain the same data value if they are connected to a power source. In this scenario, leakage current is occurring.

Read-only mode"

In this case, both access transistors M5 and M6 are connected to the bit line because the memory's content is 1. The value stored on one of the bit lines is discharged to ground to perform a read operation, while the other bit line is pre-charged via the M6 and M3 transistors. BLB must be dismissed if BLB is charged, and inversely, BLB must be charged if BLB is released. Once both inputs are delivered into the sense amplifier, the process continues.

2.3 -Writing-

We'll configure BL to store 0s and BIT to store 1s if the memory content is "0". (BLB). Setting the SR-Latch pulse is a comparable thing as doing so. The value must be stored in the latch by maintaining the Word line at a high voltage, while grounding the bit line bars to create the bit line line.

A SRAM cell is inactive when it is connected to VDD and the word line is low. The cell voltage stores the amount of power wasted in the inactive state. More than half of the power dissipation occurs via two leakage mechanisms: gate leakage and subthreshold leakage. Gate leakage is the result of hot carrier (electron and hole) injected from the source to the drain and the oxide tunnelling from the gate to the drain. In contemporary technology, leakage current in the sub-threshold range is most often seen. undervoltage under threshold leakage Subthreshold leakage current is the current which flows from the gate to the source when the gate-source voltage is lower than the threshold voltage. Weak inversion causes the same subthreshold leakage current to be generated. To reduce subthreshold leakage in an SRAM cell, the threshold voltage of the transistor must be increased. Read/write latency is increased because to the subthreshold leakage current. Reducing the write delay doesn't affect the read latency in any way.

Two-and-a-half gate tunnelling leakage

Tunneling leakage's three main components are listed below.

The gate to channel current overlaps with the gate to drain.

In this case, the width of the gate oxide is enlarged, thus increasing the field across the oxide. When the oxide thickness is lowered, the electric field is raised, and the gate tunnelling leakage occurs in the area. The gate to substrate leakage is minimal as compared to other leaks. Because of quantum mechanical tunnelling, this leak is temperature independent.

By implementing Self Controllable Voltage Level, a proposed method for reducing SG-IG SRAM leakage.

This portion uses a four-terminal Fin FET-based SG-IG SRAM for reducing leakage. Simultaneously, although independent of each other, both gates in SRAM SG are biased in IG SRAM. The TSPICE simulation required a Fin FET transistor that also has two fins with a 45nm gate length.

3.1 Device Parameter Used in Simulation

L_g (nm)	45
T_{ox} (Å)	15
T_{si} (nm)	8.4
V_{DD} (V)	1
$N_{BODY}(cm)$	2e16
H_{fin} (nm)	60
$V_{to, nmos}$	0.31

Table 1. Device Parameters

3.2 6T SRAM Cell Using SG-ULSVL

The suggested SGULSVL SRAM cell is shown in Figure 2. The bottom part of the 6T SRAM is made up of the SG-LSVL circuit, in which both gates are shorted together. The six transistors, two p-channel and one n-channel, are connected to the ground power supply and the p-channel 6T SG SRAM in this SG-LSVL. When the M10 transistor is active, it connects Vss to the 6T SRAM cell; when the M11 and M12 transistors are active, they connect Vss. 0v is supplied to the CSB, providing Vss to the SG-SRAM cell, and M10 transistor is shut off. As the virtual ground voltage lowers, so does the gate drain voltage of the M4 transistor, but at the same time, the gate source voltage of the M2 transistor is decreased, reducing the gate source voltage of the M4 transistor. There are no significant design changes to M5 and M6 transistors. Two NMOSs and a single PMOS are linked in series on the top portion

of the circuit, which is called the SG-USVL. An ON pmos transistor is attached to the power supply in the ON state, whereas an ON NMOS transistor is linked to Vdd in the ON state. Active mode functions like standby mode in that the applied voltage is kept constant. M2 and M4 transistors have their drain voltage reduced to Vdd after M3 has been activated. When the M4's gate voltage is greater than or equal to t .

The figure on the right shows the USVL and LSVL techniques combined. There are two NMOS transistors and a single pmos transistor connected above the 6T SRAM cell. Active mode involves the use of ON Pmos transistors, while standby mode features ON NMOS transistors. Reducing leakage is achieved by decreasing the supply voltage. An example of a single NMOS transistor and two PMOS transistors in series is shown below the 6T SRAM cell. When the M12 transistor is switched on and the M10 transistor is in the OFF position, six-bit SRAM will be linked to VSS.

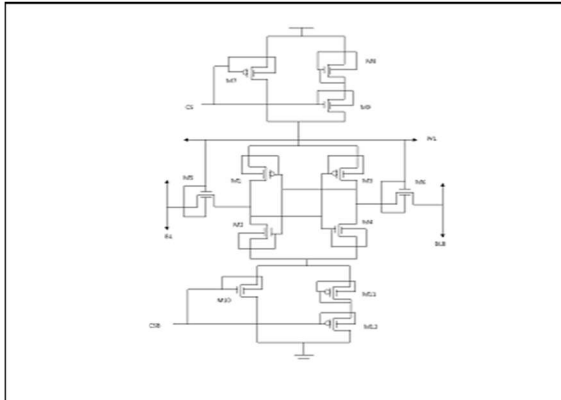


Fig2. the shortest possible ULSVL

3.3 6T SRAM Cell using IG- ULSVL

A design proposal for the IG ULSVL FinFET SRAM cell is shown in Fig. 3. USVL and LSVL are combined in this. The V_{th} of the IG Fin FIT is changed by biasing the second gate. The whole SRAM cell transistors are made up of individual gate voltage-limiting transistors. The second gate of each transistor has control lines attached to it, which is also known as the equivalent control lines. The transistor V_{th} is reduced when several operations are executed in a succession, and this is done by controlling both VG1N and VG1P. In standby mode, the V_{th} is raised to minimise leakage current. Each of the upper- and lower-level USVL circuits has two additional gates linked to the control lines VG2N and VG2P respectively.

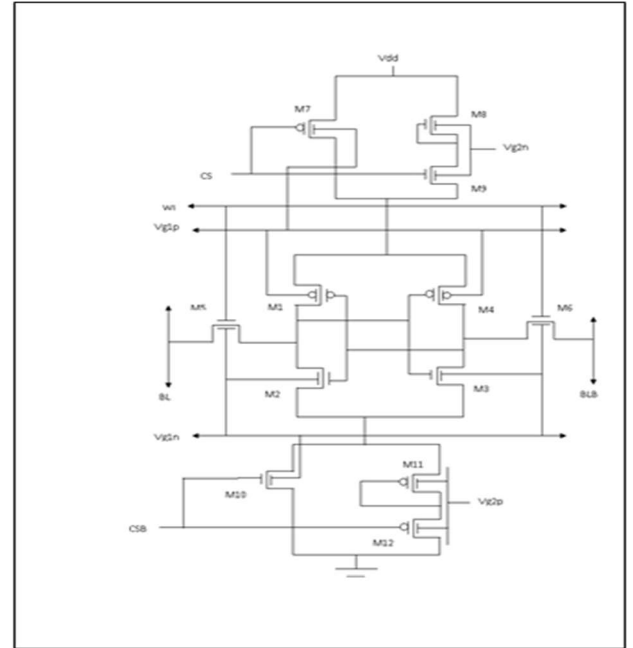


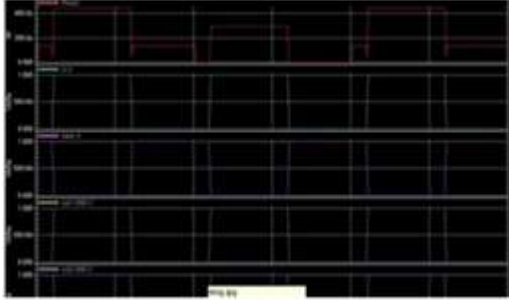
Fig3. an autonomous gate on ULSVL

A single PMOS is linked in series with the NMOS at the higher USV level (VG2N) in order to connect two NMOS. CS is connected to the M7 and M9 transistors, respectively. There are two NMOS transistors and one PMOS transistor located in the bottom left-side VLV. In order to avoid operating outside of specifications, the IG voltage of VG2P is linked to both pmos transistors, while the VG1N is connected to the NMOS transistor. The PMOS transistors are associated with the bottom part of the circuit, whereas the NMOS transistors are found in the upper half. The M10 transistor is used when in active mode, while the M11 and M12 transistors are employed while in standby mode. when no voltage is supplied to the cell, connecting the 6T SRAM cell to Vss, M10 is ON and M12 is OFF. When supplying zero voltage to the ground node, the CSB is operating in the Acti mode. There is a voltage in the M2 transistor. In the case when the upper USVL component is being used, the nmos transistors are linked to the VG2N and the PMOS transistor is attached to the VG1P. The PMOS is switched on in active mode, while the nmos is used in standby mode. mode. As the supply voltage decreases, the M4 transistor is turned ON, reducing the voltage going to M2 and M4 to Vdd. Because of the lower drain voltage, the M2 transistor has a lower gate drain voltage.

The proposed IG-ULSVL cell has a lower leakage current compared to the SG-ULSVL cell. As a consequence of higher IG voltage, the threshold voltage of the transistor is raised, decreasing SRAM cell leakage.

SIMULATION RESULTS

The conventional 6T SRAM cell simulation results and the SRAM cell with the suggested leakage reduction simulation results are provided in this section. The simulations were performed using the Tanner EDA tool, which is equipped with 45nm technology. Reduce the SRAM cell leakage by increasing the ground node voltage. These table 1 comparative findings indicate how much power SG and IG ULSVL leakage has been reduced.



This figure depicts the output waveform of a standard 6T SRAM.

By utilising LSVL and USVL, leakage may be reduced. For analysis, Jim Hawkinson gathered data showing that $8.473101e-019$ W in power and $2.339218e-019$ W in power are required to perform operations on shorted 6T SRAM cells. These 6T SRAM cells use the L VL and USVL process and leak $9.755116e-020$ W and $7.071812e-020$ W. Using these techniques, the IG 6T SRAM cells have a L akage reduction of $3.157830e-024$ W. In IG mode, a lesser leak is produced compared to in SG mode.

Table 2.		
Power Measurement		
S.N O	Techniques	power
1	Conventional 6T SRAM	$2.616419e-014$
2	SG-LSVL	$8.473101e-019$
3	SG-USVL	$2.339218e-019$
4	SG-ULSVL	$3.988957e-021$
5	IG-LSVL	$9.755116e-020$
6	IG-USVL	$7.071812e-020$
7	IG-ULSVL	$3.157830e-024$

3. CONCLUSION

This study discusses the various parameters of a FinFET-based 6T SRAM cell. Because SRAM cells play such a significant role in embedded system designs, they should have lower leakage power in order to give greater performance as technology evolves. In SG-IG mode, the SVL approach is employed to reduce cell leakage. While the Independent gate LSVL and USVL methods are superior in terms of reducing sub-threshold leakage current and gate leakage current, the Independent gate LSVL and USVL methods are better in terms of reducing gate leakage current.

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