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Reversible Gate Logic Adder with Parity Preserving Design

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Abstract:

Reversible logic circuits have drawn attention from a variety of fields, including nanotechnology, optical computing, quantum computing, and low-power CMOS design. Low-power and high-speed adder cells (like the BCD adder) are used in binary operation-based electronics. The most fundamental digital circuit activity is binary addition. It serves as a foundation for all subsequent mathematical operations. The main challenge today is to reduce the power consumption of adder circuits while maintaining excellent performance over a wide range of circuit layouts. Error detection in digital systems is aided by parity preservation. This article proposes a concept for a fault-tolerant parity-preserving BCD adder. To reduce power consumption and circuit quantum cost, the proposed method makes use of reversible logic gates like IG, FRG, and F2G. Comparing the proposed circuit to the current counterpart, it has fewer constant inputs and garbage outputting devices and is faster.

Keywords — **BCD** Adder, Reversible Logic, Double Feynman Gate, Islamic Gate (IG)

1. INTRODUCTION

When a system's components fail, fault tolerance enables it to continue working as intended. Fault detection and repair are made simpler and more easy when the system is designed using fault-tolerant components. Fault tolerance in communication networks and other systems may be achieved using parity, which is a mathematical concept. As a consequence, parity-preserving reversible circuits will be the future design trend in nanotechnology for fault-tolerant reversible systems. To be parity-preserving, a gating network's component gates must all be parity-preserving. Several parity-preserving logic gates have been proposed in the literature. Reversible logic gates are parity-preserving if the EX-OR of their inputs matches the EXOR of their outputs, which is the case in most applications. Parity-preserving reversible logic gates such as the Islamic Gate (IG), Double Feynman Gate, F2PG, and PPPG are important in this context. The Fredkin gate is a parity-preserving reversible logic gate.

A. Double Feynman Gate (F2G)

Figure 1 depicts a 3*3 Double Feynman gate. The input vector is represented by A, B, and C, while the output vector is represented by O. (P, Q, R). It is possible to express the outputs as follows: P=A, Q=A or B and R=AxorC. The quantum cost of the double Feynman gate is two.

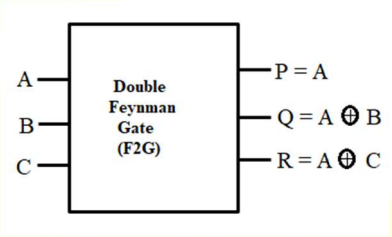

Fig 1: Double Feynman Gate

B. Fredkin Gate

On Fig. 2, we can see a 3x3 Fredkin gate. The input vector is represented by A, B, and C, while the output vector is represented by O. (P, Q, R). When P=A, then Q=(A'B) xor (AC), and R=(A′C) xor (AC), then the output is defined as (AB). The quantum cost of a Fredkin gate is 5. The logic circuit shown in the figure utilises a 3x3 gate. A five-quantum price tag is attached to this item's sale price. You may use it to build a Multiplexer. Two multiplexers have been switched (permuted) from the same control input A to create this gate.

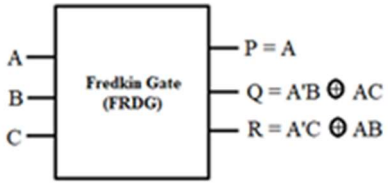

Fig 2: Fredkin Gate

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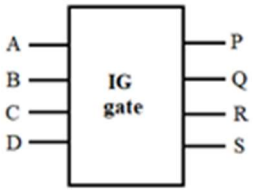
C. IG GATE

Figure 3 shows the IG gate, which has 44 inputs (A, B, C, and D) and outputs (P, Q, R, and S). The binary values are as follows: P = A, Q = A⊕B, R= AB⊕C and S = BD⊕B′(A⊕D).



You can see here how the paper is organised. Section II describes the related work on the design of a reversible logic BCD adder, and Section III discusses the proposed work. The design implementation and simulation results are found in Section IV. The conclusion is found in Section V. Ingress and Exit Control (Figure 3)

2. RELATED WORKS

Thapliyal suggested a novel ripple carry adder with a shorter logic depth (delay) than current equivalents for the amount of input bits and garbage outputs. The authors of the study are H, et al. There is a new architecture for efficient Binary Coded Decimal (BCD) addition/subtraction developed by Anshul Singh et al. [2] that does not need any additional hardware. If a number is positive or negative, it is accepted by the architecture in any case. In terms of gates and garbage outputs, A.K. Biswas et al.[3] provide efficient techniques for BCD adder adders. F. Naderpour et al. [4] developed a novel reversible BCD adder with the goal of reducing circuit depth. Members of the research team led by Professor Ashish Kumar Biswas. A method for rapid addition of decimals (QAD) suited for multi-digit BCD addition utilising reversible conservative logic was presented by James, R.K. Shahana, and others (2007). Theodore K. Only Fredkin gates that are both fault tolerant and reversible are used in the design. Reversible halves and full adders for binary integers n bits and BCD numbers m bits have been proposed by M.K. Thom and R. Gluck[7]. H.M.H. Babu and A.R. Chowdhury originally proposed a reversible binary coded decimal (BCD) adder in reversible logic synthesis [8]. Reversible logic adders such as Himanshu Thapliyal et al. [9]'s conventional BCD adder and carry skip BCD adder are built utilising TSG gates.

According to a review of the literature, a significant amount of work has been done on reversible computing for low-power computers. Developing an efficient and fault-tolerant parity-preserving BCD Adder is the main goal of this research. In addition to building the circuit, you'll need to use as few reversible gates as possible to minimise garbage outputs while simultaneously reducing the amount of constant inputs. Reduced trash means the gadgets are simpler, which would indicate a decrease in trash production. As technology becomes smaller, there's less switching going on, which lowers power consumption while also boosting performance. Complex ALU circuits may be powered using a high-performance energy-efficient cell that uses very little power.

The BCD Adder as an example

For instance, the sum-to-total BCD 1-digit adder simultaneously adds two BCD digits while also generating the Sum BCD digit and the required correction logic. A BCD adder is a combinational circuit that adds two BCD numbers together. Binary coded decimal numbers are required for the BCD adder to work. Two 4-bit binary integers are given as input and one number is returned. Both inputs must be between the range of 0000(0) to 1001 (9). So we'll know in a couple of hours or so how many people passed. Adding 0110(6) to the original total is required for BCD adder sums higher than 9. Because of this, the traditional BCD adder is both larger in power consumption and slower. The input carry Cin is represented by C0 in the current design of the reversible BCD adder [10], the carryout of the 4 bit reversible binary adder is represented by OC, and the output carry of the 1 digit BCD adder is also represented by OC. As of now, there is just one ancilla input bit and no trash outputs in the present reversible BCD adder architecture. Quantum cost of 70 is suggested for an input-carry reversible BCD adder. Increased complexity and a large number of reversible gate variants limit the current BCD reversible adder.

3. PROPOSED BCD ADDER

Keeping the Scales Equal Parity reversible gates are used in the BCD Adder. The BCD Adder performs the job, however for data transmission the parity-preserving BCD Adder is safer. Reversible logic gates with parity preservation have the property that the input and output parities are the same. We build a parity-maintaining BCD adder with reversible gates. Figure 4 depicts the three-phase design process for a BCD adder. Parity-preserving reversible gates like the

IG gate are used in the first step to construct the whole adder circuit. For installation, you'll need two IG gates. The IG gate may be used to construct a 4-bit ripple carry adder by cascading the adder circuits in second ste.

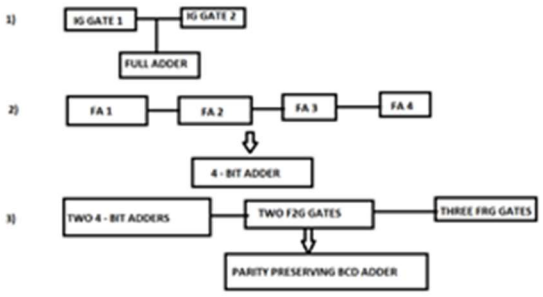


Fig. 4: Flow chart for the BCD Adder Design

Unlike a conventional BCD adder, which is built using the same concept, the suggested design uses logic realisation that incorporates parity reversible gates in the third stage of the BCD adder's construction. A result of the logic reduction called for the employment of three Fredkin gates, two Feynman double gates, and two ripple carry adders with a carry of four bits.

A full adder with an IG gate.

The full adder circuit is used to add three-bit binary integers, and the usual Boolean statement is:

Sum = A ⊕ B ⊕Cin

Carry = (A ⊕ B) Cin⊕ AB

As shown in Figure 5, the IG gate-based strategy is used. Because of this, two IG gates are used in the design, each of which includes two logic 0 constant sources and three garbage sources in addition to the required inputs and outputs.

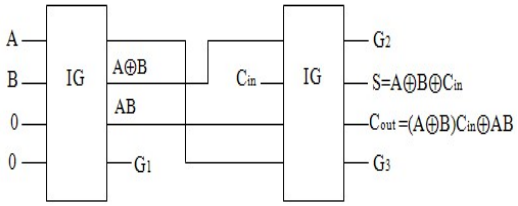


Fig 5: As a Full Adder, use two IGs.

The expressions for garbage outputs: G 1= B′ A, G2 = A⊕ B and G3 = Cin A ⊕Cin′ B.

B. Design of 4-Bit Ripple Adder

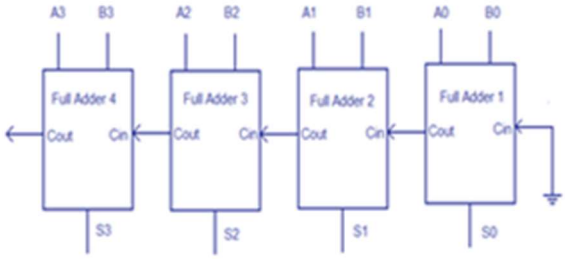


Fig 6: Block diagram of 4-Bit Ripple Adder

A four-bit ripple carry adder design is shown in Figure 6 (below). As seen in Figure 5, it makes use of four proposed full adders (Fig. 5), each of which contains eight consistent input values as well as twelve garbage output values.

C. Parity preserving BCD Adder

Reversible logic gates with parity preservation have the property that the input and output parities are the same. For the parity-preserving BCD adder shown in figure 7, the proposed 4-bit ripple carry adder is combined with a few additional parity-preserving reversible gates. This creates two 4-bit ripple carry adders as well as two Feynman double gates and three Fredkin gate elements.

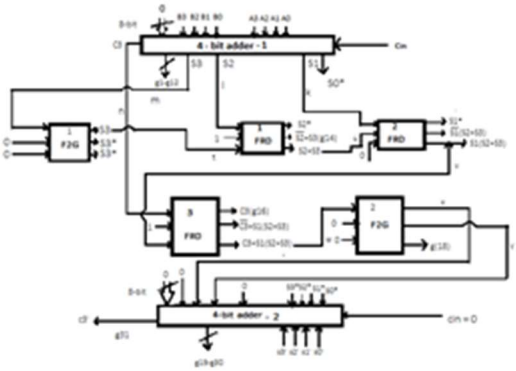


Fig. 7: Proposed BCD Adder with Parity Preservation

The following is a description of how each module in the proposed BCD adder works.:

(i) 4-BIT RIPPLE ADDER-1

The block uses two 4-bit binary numbers known as BCD numbers, which are designated A and B. These two inputs are sent into a 4-bit parity-preserving reversible adder, which also receives an 8-bit constant input of logic 0. This 4-bit adder's input carry is considered to be 0. The 4-bit adder's outputs are designated s3,s2,s1,s0*, while the remaining outputs are garbage values labelled g1-g12.

(ii) F2G -1

One of the inputs of F2G-1 is S3 of 4-bit adder -1, while the other two are default 0. S3,s3*, and s3* are the three inputs..

(iii) FRD-1
One of the inputs is S2 from the 4-bit adder1, while the second input is S3 from F2G1. By default, the third input is 1. As a result, the FRD-1 outputs are s2*,s2+s3(g14),s2+s3(g14),s2+s3(g14),s2+s3(g14),s2+s3(g14.
(iv) FRD-2
One of the inputs for FRD-2 is S1 from 4-bit adder-1, another input is FRD-1's output s2+s3, and the third input is 0 by default. As a result, the FRD-2 outputs are s1*,s1(s2+s3),s1(s2+s3).
(v) FRD-3
One of the inputs of FRD-3 is C3, another is FRD-2's output s1(s2+s3), and the third input is the default 1. As a result, the FRD-3 outputs are c3(g16), c3+s1(s2+s3), and c3+s1(s2+s3).
(vi) F2G-2
One of the inputs of F2G-2 is the FRD-3 output C3+S1(S2+S3), while the other two are left blank. X,Y,g are the F2G-2 outputs (18).
(vii) 4-BIT RIPPLE ADDER-2
The two F2G-2 outputs X,Y are supplied as inputs, together with s3*,s2*,s1*,s0*,0,0. The sum and carry output of the 4-bit adder-2 will be obtained.
It can be seen from the architecture that the number of inputs equals the number of outputs, which follows the reversible principle.

4. EXPERIMENTAL RESULTS

In order to synthesise the proposed BCD adder, Xilinx's ISE simulator was used, and Mentor Graphics' Modelsim-SE was used for simulation. Figures 8 to 10 show the simulation of the proposed adder's individual blocks in action.

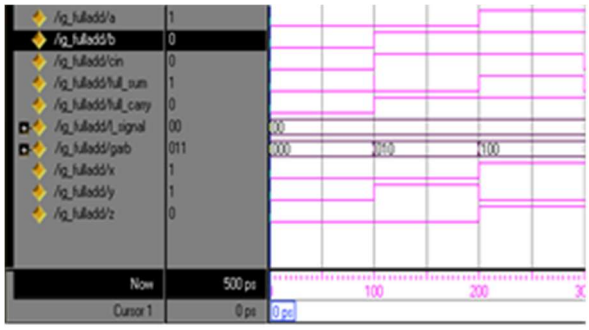


Fig 8: IG Gate as a Full Adder

Fig. 9: 4-Bit Adder using IG Gate as Full Adder

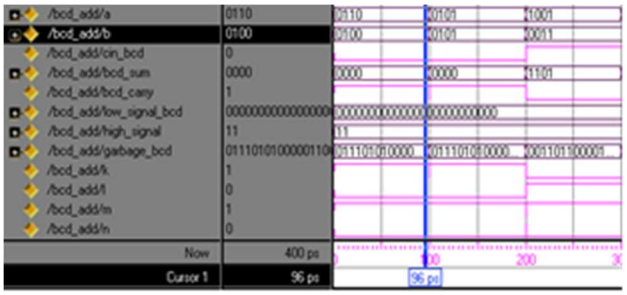


Fig 10: Parity Preserving BCD Adder

The number of input and output lines is equal, and the outcomes are also fulfilled for each operation, according to simulation findings..

5. CONCLUSION

Because we live in a world dominated by mobile technology, the most important trend in electronics right now is increased power consumption. The study's primary objective was to learn more about Reversible Computation and how it might be utilised to improve the energy efficiency and lifespan of electronic equipment. The BCD Adder is a fundamental computer arithmetic circuit module. Because of this, it's the most power-hungry part of the BCD Addition. Reversibility was considered while designing a parity-preserving BCD Adder circuit that made use of the fault-tolerant gates Fredkin, F2G, and IG already in place.

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